**ECE 501 ASSIGNMENT 6: SHIFTER**

**Roshni Uppala**

**1011735230**

*Objective : To design a 8-bit barrel shifter that shifts the amount specified in the input for each block in one clock cycle. Also to develop its control unit which would instantiate the shifter along with some other considerations.*

**Design Specification :**

* Inputs :
* Data in – 8 bits
* Clear 1 bit – high (1) when register is cleared
* Load 1 bit – high (1) when data is to be loaded into the register
* Clock 1 bit – continuous square wave with 40nS period
* Amount 3 bits – the number of shifts to be taken
* Shift type 2 bits – the type of shift to be made

0 – no shift

1 – left shift circular

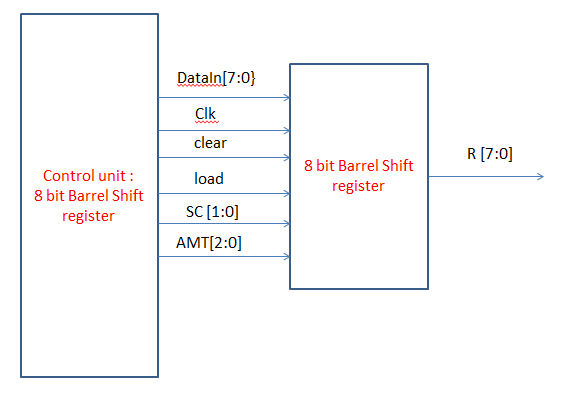
2 – right shift logical

3 – left shift logical

* Outputs :
* Data out – 8 bits
* Functional behavior :
* Load data in parallel and then shift the number of positions specified by Amount in the direction and manner specified by Shift Type
* Stop shifting the data even if the clock continues.
* Data, shift type, and amount will only be present while the load signal is present
* Load will be high for one clock cycle
* Complete the shift with one clock rising edge

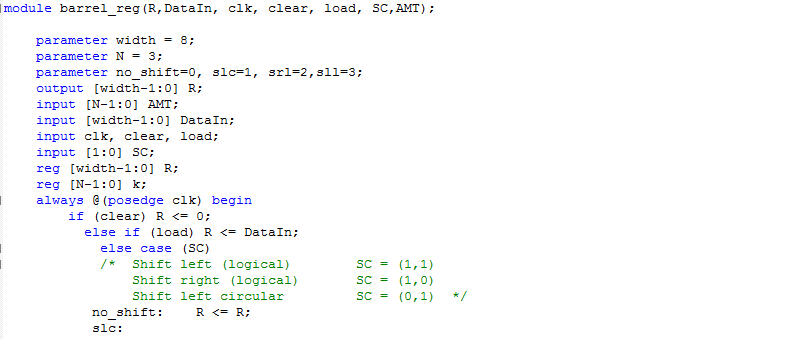
**Design Structure :**

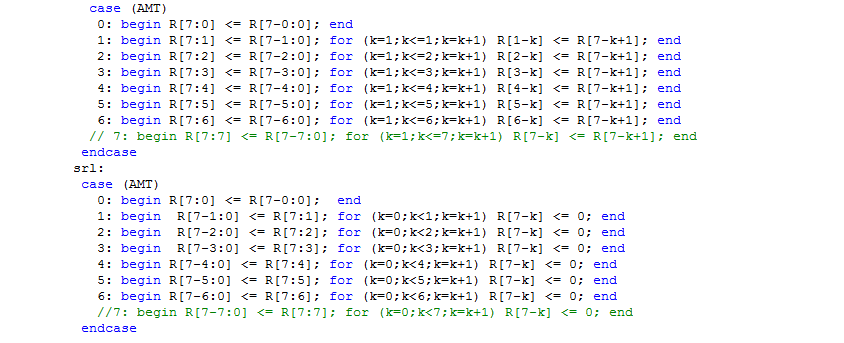
* Inputs :
* Datain – 8 bits data input at every 100ns.
* AMT – 3 bits , specifying the amount the bits are to be shifted.
* Amount – 3 bit register which saves the AMT value
* SC- 2 bit , specifying the type of shifting to be performed.
* Shifting\_type- 2 bit register, stores the value of SC.
* Clock – Clock is given at every 20 ns. ( high at every 20 ns )
* Load – load signal is given for a clock period.
* Clear- clear is given at the beginning to clear the registers.
* Outputs :
* R[ 7:0] – 8 bits data out
* Functional behavior:
* Clear data in register
* Load data in register
* Load data in parallel and then shift the number of positions specified by Amount in the direction and manner specified by Shift Type
* Stop shifting the data even if the clock continues. Shifts are sequential.
* Data, shift type, and amount will only be present while the load signal is present
* Load will be high for one clock cycle
* Complete the shift with one clock rising edge
* Shifts are sequential and complete their shift in one clock
* The control inputs are srl, sll, and shc along with the number of bits to shift.

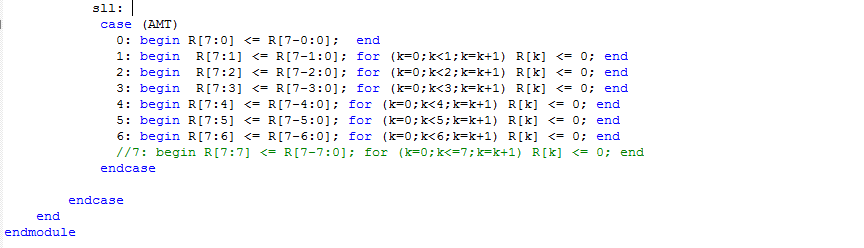


*Fig 6.1 : design structure of the 8 bit barrel shifter , shifting in one clock period*

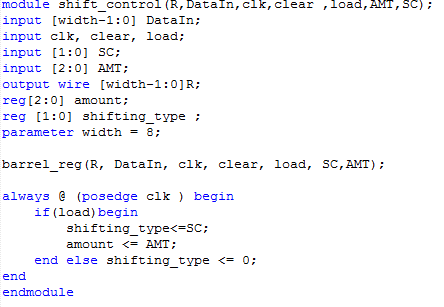
* **Design Entry :**
* Verilog code :





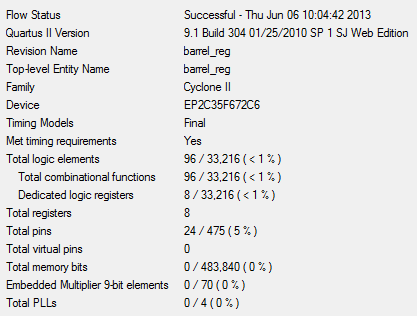
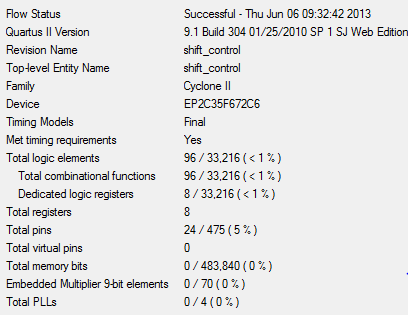


*Fig 6.2 : Verilog code for 8-bit barrel shifter*



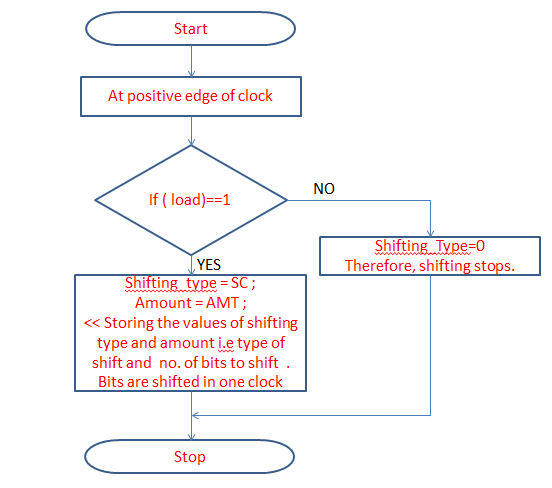
*Fig 6.3: Control unit for 8-bit barrel shifter*

* Compilation report:



*Fig 6.4: Compilation report ,left : Shift control , right: barrel shift register*

* Flowchart of control unit:



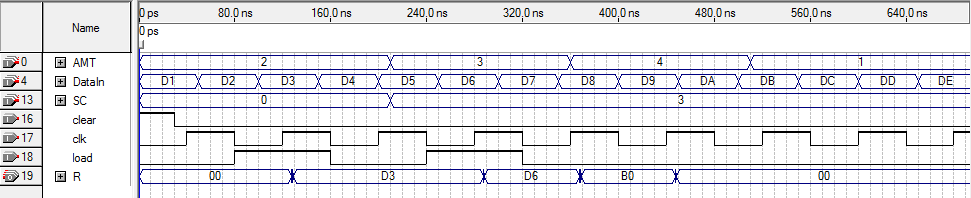
*Fig 6.5: Flowchart*

* **Design verification :**

Test Plan :

The different input values are given to datain , shifting type is specified at SC, shifting amount is specified at AMT. The data in is maintained at 100ns. The load is given at the rising edge of the clock. The clock goes high for every 20ns.

Test 1: No shifting and left logical shift



I Clock Period

I Clock Period

Load high but negative clock, so value D6 is loaded but noshifting.

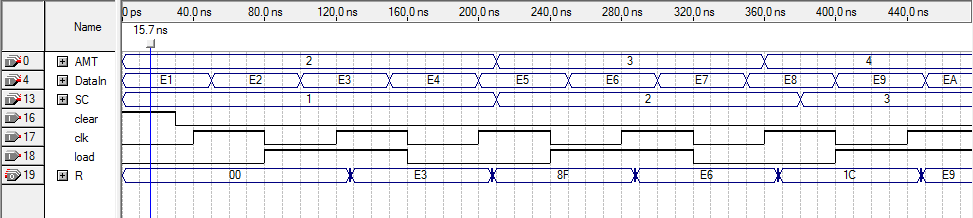
Negative clock, one clock period is complete, shift is complete, therefore shift stops.

D3 is loaded , no shift , so D3 stays

D6 is loaded , shift type is sll with AMT = 4 . Ans = 10110000 = B0

*Fig 6 .6: No shifting and left logical shift 8-bit barrel shifter*

Test 2 : Left shift circular and right logical shift



I Clock Period

I Clock Period

E3 is loaded , shift type is SLC with AMT = 2 . Ans =10001111= 8F

E6 is loaded , shift type is SRL with AMT = 3 . Ans = 00011100 = 1C

*Fig 6.6: Left circular and right logical shift shift 8-bit barrel shifter*

**Result :**

*Hence, the 8 bit barrel shift register has been designed with a control unit which would instantiate it and complete the shifting process in one clock cycle. The Test simulation results are mentioned. The only disadvantage in the barrel shift register of fig 6.2 encountered is that for AMT = 7 , the shift register sometimes works and sometimes doesn’t. It should probably be the error of the software. Otherwise, the shifting process is successfully achieved for the desired amount of bits and for the desired shifting type and is completed in one clock cycle. The control unit stops the shifting process when the desired shift amount is reached.*